REMARKS

Applicant has amended claim 1 for purposes of clarity so that it is clear that the plurality of bond pads are formed in the substrate. Although the Examiner may very well have presumed this to be the case, it is necessary to have claim 1 amended to avoid any misinterpretation of where the bond pads are located. Since this is a clarification of the claim, Applicant believes the claim should be entered even if the Examiner does not consider the claim to be in condition for allowance.

Applicant's invention is directed to a packing process for a semiconductor package. In the first step, a plurality of conductive bumps each having a flat end is formed on a chip mounting area of a substrate by screen printing, such that the conductive bumps are in direct alignment over a plurality of bond pads formed in the substrate and electrically connected to the substrate. Next, a first encapsulant is formed by printing to encapsulate the conductive bumps, such that the flat ends of the conductive bumps are exposed and level with a top surface of the first encapsulant. Then, a chip is mounted on the first encapsulant, allowing bond pads formed on the chip to be electrically connected to the exposed ends of the conductive bumps. Finally, a second encapsulant is formed on the substrate to encapsulate the chip. This packaging process assures no gap left between the chip and the first encapsulant, thereby preventing void formation or popcorn effect from occurrence.

Applicant respectfully traverses the rejection of claims 1-3, 5, 6 as being unpatentable over Booth (US 5,543,585) in view of Applicant's admitted prior art (AAPA) and Takeuchi et al for the reasons given below and that the cited references fail to teach or suggest forming a plurality of bond pads in the substrate.

Booth et al is cited as teaching Applicant's packaging process for a semiconductor package. However, it is self-evident from Figs. 5 and 6 of Booth et al that Booth does not teach or suggest forming the bond pads in the substrate i.e. internal of the substrate. Instead, it is evident from Figs. 5 and 6 that conductive pads 8 are formed on the substrate 1 before the conductive adhesive bumps or pegs 4 are applied by mask screening on the conductive pads 8. Accordingly, the conductive adhesive bumps or pegs in Booth et al are not designed to be in direct alignment or to lie in a coplanar surface due to a step difference created by locating the

conductive pads 8 on the substrate which will inherently cause misalignment to occur during the mask printing. On the other hand, the conductive pads in amended claim 1 are now emphasized as being formed in the substrate. Therefore, the packaging process disclosed by Booth et al is readily susceptible to misalignment and does not teach a substrate with a plurality of bond pads in the substrate.

Applicant's admitted prior art (AAPA) is also cited in the office action to teach encapsulating the chip and implanting the solder balls to the opposite side of the substrate. Takeuchi is cited as evidence that mask screening as taught in Booth et al is the same as screen-printing in Applicant's invention. However, Applicant does not find any supporting evidence from both APA and Takeuchi for teaching or suggesting forming the conductive pads in the substrate. Therefore, even if Booth et al is combined with the AAPA and Takeuchi, the combination still fails to teach a coplanar surface between the conductive bumps and the first encapsulant, such that flat ends of the conductive bumps are exposed level with a top surface of the first encapsulant to prevent misalignment during screen-printing of the conductive bumps. This is a significant distinction which the Examiner continues to overlook. For the foregoing reasons, Applicant respectfully submits claim 1 patentably distinguishes over the cited references. Claims 2-3 and 5-8 respectively depend from claim 1 and are patentable for at least the same reasons.

The rejection of claim 7 over Booth et al, AAPA, Takeuchi et al and Cook et al (USP 6,331,446) is respectfully traversed. The Examiner allegedly states that it is obvious to combine a second encapsulant that forms a fillet around the edges of the chip without encapsulating the outer surface of the chip from the combined teachings of all of the cited prior art references. However, as is clearly disclosed in Cook et al, the material (26) is an underfill material used to enclose and seal the other underfill material (24). Further, it is stated in Cook et al (Col. 1, lines 60-62), that the release of moisture during the underfill process may create voids in the underfill material, and that the bumps may extrude into the voids during thermal loading, particularly for packages with a relatively high bump density (Col. 2, lines 3-5). Similarly, Applicant's admitted prior art also discusses the problem created as a result of the underfill process. Clearly, the prior art and Applicant's admitted prior art associates the underfill process with voids and gap formations. On the other hand, the present invention clearly teaches a

package process which does not use any underfill process and that no gap is formed between the chip and the substrate. For the reason listed above, it is not obvious to combine the cited references since the cited references all clearly emphasize the need to use the underfill process thereby admitting the necessity for a step which the subject invention eliminates as a result of the claimed arrangement. How then can the claimed arrangement be obvious?

Moreover, the rejection made by combining Booth et al, AAPA, Takeuchi and Lai et al (USP 6,323,066) is also traversed based on the fact that none of the cited references teach or suggest forming the conductive pads in the substrate.

For all of the above reasons, applicant clearly believes claim 1 and the dependent claims 2, 3 and 5-8 are clearly patentable over all of the cited references taken individually or in combination.

Reconsideration and allowance of claims 1-3 and 5-8 is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

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1. (Currently Amended) A packaging process for a semiconductor package, comprising the steps of:

1) preparing a substrate having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface with the first surface having a first plurality of bond pads formed in the substrate and are electrically connected to the substrate;

2) screen printing a plurality of conductive elements on the chip-mounting area of the substrate in direct alignment over each of said first plurality of bond pads, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant by a printing process on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant formed by printing is adapted to have a top surface thereof formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant;

4) preparing at least one semiconductor chip having a second plurality of bond pads formed on a surface thereof, and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the second bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface;

5) forming a second encapsulant on the first surface of the substrate for encapsulating the chip; and

6) implanting a plurality of solder balls on the second surface of the substrate, wherein the solder balls are electrically connected to the substrate.

2. (Original) The packaging process of claim 1, wherein the conductive elements are conductive bumps.

3. (Original) The packaging process of claim 2, wherein the conductive bumps are made of tin, lead or tin/lead alloy.

4. (Cancelled)

5. (Cancelled)

6. (Original) The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon encapsulated by the second encapsulant.

7. (Original) The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon exposed to the outside of the second encapsulant for directly contacting the atmosphere.

8. (Previously Amended) The packaging process of claim 1, further comprising a step of attaching a heat sink to the first surface of the substrate after the step (4) of mounting the chip on the first encapsulant, allowing the heat sink to be encapsulated by the second encapsulant in the step (5) of forming the second encapsulant.